

**FSA MIXED-SIGNAL/RF  
PDK CHECKLIST**
**Checklist Form**  
Version 2.0

**Foundry and Support Contact Information**

Foundry           austriamicrosystems  
Process           S35xx (Cadence HIT-Kit v3.70)  
Date               08/2007

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**Foundry Process Documents**

Document	Document Number & Title	Section	Revision	Date
Design Manual (Devices)	-See individual documents below			
Electrical Parameters	ENG-219: S35 Process Parameters ENG-308: S35 12V HBT Module PP		4.0 1.0	Dec 2005 Oct 2006
Design Layout Rules	ENG-218: S35 Design Rules ENG-309: S35 12V HBT Module DR ENG-42: Standard Family Cells		5.0 2.0 3.0	Nov 2004 Jan 2007 Feb 2007
SPICE Model Library	ENG-219: S35 Process Parameters	4	4.0	Dec 2005
SPICE Model Checklist	FSA Spice Model Checklist S35		1.2	Aug 2007
RF Parameters/Modeling	ENG-221: S35 RF Spice Models		3.0	Nov 2005
Noise Model	ENG-225: S35 Noise Parameters		2.0	Jan 2007
Matching Models	ENG-223: S35 Matching Parameters		2.0	May 2006
ESD Guidelines	ENG-236: 0.35u ESD Design Rules		1.0	Jun 2003
DRC	ENG-218: S35 Design Rules	4	5.0	Nov 2004
LVS	ENG-218: S35 Design Rules	5	5.0	Nov 2004
Parasitic Extraction	ENG-219: S35 Process Parameters		4.0	Dec 2005
Layer Map	ENG-218: S35 Design Rules	3	5.0	Nov 2004

## EDA Tools Supported and Verified for Use with this PDK

Type	Vendor and Tool	Version	Version Date
Schematic	Cadence Composer	IC 5.1.41 USR4	Jul 2005
Simulation Control	Cadence Analog Design Environment	IC 5.1.41 USR4	Jul 2005
Circuit Simulator (A)	Cadence Spectre	IC 5.1.41 USR4	Jul 2005
	Cadence Ultrasim	MMSIM6.0	Jul 2005
	Mentor Eldo	6.5.2	Jul 2005
	Synopsys HSpice	2004.03SP1	Jul 2005
	Agilent ADSSim	2004A	Jul 2005
Circuit Simulator (B)	Synopsys HSIM	5.0	Jul 2005
	Silvaco SmartSpice	2.0.8.C	Jul 2005
	Cadence PSPICE	9.2	Jul 2005
	Dolphin Smash	4.3.5	Jul 2005
	Synopsys Saber	4.3	Jul 2005
Circuit Simulator (C)			
Circuit Simulator (D)			
Layout Editor	Cadence Virtuoso-XL	IC 5.1.41 USR4	Jul 2005
	Cadence Chip Assembly Router	ICC 11.2	Jul 2005
DRC Checker	Cadence Assura	3.1.5	Jul 2005
	Mentor Calibre	2006.4	Jul 2005
LVS Checker	Cadence Assura	3.1.5	Jul 2005
	Mentor Calibre	2006.4	Jul 2005
Parasitic Extractor	Cadence Assura	3.1.5	Jul 2005
	Mentor Calibre	2006.4	Jul 2005
Analysis Tools	Cadence VoltageStorm		Jul 2005

## Device Tables

Device Type	Device Name	Comment	Terminals	Symbol	Sim-Net-A	Sim-Net-B	Sim-Net-C	Sim-Net-D	LVS Net	SDL Net	GDS	P-Params	Sim-Test-A	Sim-Test-B	Sim-Test-C	Sim-Test-D	DRC Test	LVS Test	P cell Test	Extract Test
MOS	nmos4		4	✓	✓				✓	✓	✓	10	✓	✓			✓	✓	✓	✓
	pmos4		4	✓	✓				✓	✓	✓	10	✓	✓			✓	✓	✓	✓
	nmosm4		4	✓	✓				✓	✓	✓	10	✓	✓			✓	✓	✓	✓
	pmosm4		4	✓	✓				✓	✓	✓	10	✓	✓			✓	✓	✓	✓
	nmosh4		4	✓	✓				✓				✓	✓			✓	✓		✓
	nmosmh4		4	✓	✓				✓		✓		✓	✓			✓	✓		✓
	nmosrf	1	4	✓	✓				✓	✓	✓	9	✓				✓	✓	✓	✓
	pmosrf	1	4	✓	✓				✓	✓	✓	9	✓				✓	✓	✓	✓
	pldmos		4	✓	✓				✓	✓	✓	9	✓				✓	✓	✓	✓
BJT	vert10		4	✓	✓				✓	✓	✓		✓	✓			✓	✓		✓
	lat2		5	✓	✓				✓	✓	✓		✓	✓			✓	✓		✓
	npn111		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn121		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn132		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn143		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn232		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn243		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn254		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn111h5		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn121h5		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn132h5		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn143h5		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn232h5		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn243h5		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn254h5		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn221h12		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn232h12		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
	npn243h12		4	✓	✓				✓	✓	✓	1	✓	✓			✓	✓	✓	✓
Diode	nwd	2	2	✓	✓				✓	✓	✓		✓	✓			✓	✓		✓
	subdiode	2	2	✓	✓				✓	✓	✓		✓	✓			✓	✓		✓
	welldiode	2	2	✓	✓				✓	✓	✓		✓	✓			✓	✓		✓
CAP	cpoly		2	✓	✓				✓	✓	✓	6	✓	✓			✓	✓	✓	✓
	cpolyrf		3	✓	✓				✓	✓	✓	8	✓				✓	✓	✓	✓
	cmim		2	✓	✓				✓	✓	✓	4	✓	✓			✓	✓	✓	✓
	cmimrf		3	✓	✓				✓	✓	✓	4	✓				✓	✓	✓	✓
	csink		2	✓	✓				✓	✓	✓	2	✓	✓			✓	✓	✓	✓
	ctact		2	✓	✓				✓	✓	✓	2	✓	✓			✓	✓	✓	✓

## Comments

- 1 Device physically identical with standard MOS device but with fixed gate length of 0.35µm
- 2 Diode devices simulation models only for use under reverse bias conditions

Cadence Diva also supported for DRC, LVS and parasitic extraction for all devices but not classed as "Golden"

## Device Table Continued

Device Type	Device Name	Comment	Terminals	Symbol	Sim-Net-A	Sim-Net-B	Sim-Net-C	Sim-Net-D	LVS Net	SDL Net	GDS	P-Params	Sim-Test-A	Sim-Test-B	Sim-Test-C	Sim-Test-D	DRC Test	LVS Test	Pcell Test	Extract Test
RES	rpoly1		2	✓	✓				✓	✓	✓	9	✓	✓			✓	✓	✓	✓
	rpoly2		2	✓	✓				✓	✓	✓	9	✓	✓			✓	✓	✓	✓
	rpoly2rf		3	✓	✓				✓	✓	✓	10	✓				✓	✓	✓	✓
	rpolyb		2	✓	✓				✓	✓	✓	9	✓	✓			✓	✓	✓	✓
	rpolybrf		3	✓	✓				✓	✓	✓	10	✓				✓	✓	✓	✓
	rpolyh		2	✓	✓				✓	✓	✓	9	✓	✓			✓	✓	✓	✓
	rpolyhrf		3	✓	✓				✓	✓	✓	10	✓				✓	✓	✓	✓
	rnwell		3	✓	✓				✓	✓	✓	9	✓	✓			✓	✓	✓	✓
	rdiffp		3	✓	✓				✓	✓	✓	9	✓	✓			✓	✓	✓	✓
	rdiffn		3	✓	✓				✓	✓	✓	9	✓	✓			✓	✓	✓	✓
IND	SPxx	3	3	✓	✓				✓	✓	✓		✓				✓	✓		✓
	DIxx	4	4	✓	✓				✓	✓	✓		✓				✓	✓		✓
VAR	cvar		3	✓	✓				✓	✓	✓	2	✓	✓			✓	✓	✓	✓
	ivar		3	✓	✓				✓	✓	✓	2	✓	✓			✓	✓	✓	✓

## Comments

- 3 PDK contains a library of 43 fixed geometry inductors  
 4 PDK contains a library of 10 fixed geometry differential inductors

Cadence Diva also supported for DRC, LVS and parasitic extraction for all devices but not classed as "Golden"

## IMPORTANT DISCLOSURES

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