Slew-Rate Controlled Output Buffer
BU8SRC

Process

C35 (0.35µm)

Key Features

- Pad-limited 52.762 mil² / 34040 µm²
- EMC optimized Output Buffer
- Selectable slew-rate (four slew-rates possible)
- Ability of changing the slew-rate during operation of the integrated circuit
- No crowbar current of the output transistors
- Optimized di/dt for low radiated and conducted electromagnetic emissions
- Distributed and weighted technique
- Over- and undershoot (ringing) reduction
- Reduction of the high frequency spectral content
- Selected slew-rate is independent of the slew-rate of the input signal
- Dynamic switching current optimized
- Available in C35B3 (3 metal) and C35B4 (4 metal)

Description

The BU8SRC is a Slew-Rate Controlled (SRC) pad-limited output buffer with 8mA drive strength. It offers significant reductions of the conducted and radiated electromagnetic emissions of integrated circuits. With the two Slew-Rate Control Input Pins (St0 and St1) the slew-rate of the output signal can be adjusted in four different values:

St0 = St1 = 0 => slew-rate 1 (highest)
St0 = 1 / St1 = 0 => slew-rate 2
St0 = 0 / St1 = 1 => slew-rate 3
St0 = St1 = 1 => slew-rate 4 (lowest)

The slew-rate can be set to a fixed value, or it can be varied during the operation by simply changing the values of the two Slew-Rate Control Input Pins. In addition to the BU8SRC output buffer with selectable slew rates there are also four versions available with fixed slew rates (BU8SRC_00, BU8SRC_01, BU8SRC_10, and BU8SRC_11).
Using these output buffers the ground bounce amplitude as well as the ringing of the output signal can be reduced significantly. They should be used in designs where the reduction of the electromagnetic emission as well as the signal integrity of integrated circuits is of interest.

Pinlist

Pin	Description	Typ	Cap
A	Input	DIN	0.037pF
PAD	Output	DOUT	
St0	Slew-Rate Control Input	DIN	0.005pF
St1	Slew-Rate Control Input	DIN	0.005pF

Symbol

DC Characteristics

Cell Name	Vol [V]	Voh [V]	Iil [mA]	Iih [mA]	Note
BU8SRC	0.4	2.5	8	8	1)

1) Temperature range - 40°...125°C, VDD = 2.97V (3.3V – 10%), Worst Case Speed Process

Power Dissipation

St 1	St 0	Power
0	0	23.14µW/MHz
0	1	27.75µW/MHz
1	0	31.77µW/MHz
1	1	33.58µW/MHz

AC Characteristics

The AC Characteristics depend on the setting of the Slew-Rate Control Input signals St0 and St1.
Delay [ns] = f(SL, L), Output Slope [ns] = f(SL, L) with SL = Input Slope [ns] and L = Output Load [pF]
Tj = 25°C, VDD=3.3V, Typical Process

Case A: St0 = 0 / St1 = 0

	Rise				Fall			
Slope [ns]	0.1		2		0.1		2	
Load [pF]	20	600	20	600	20	600	20	600
Delay A => PAD	12.21	45.60	12.34	45.88	13.31	52.05	13.51	52.14
Slew A => PAD	14.97	58.19	14.70	58.26	12.87	70.17	12.63	70.16

Case B: St0 = 1 / St1 = 0

	Rise				Fall			
Slope [ns]	0.1		2		0.1		2	
Load [pF]	20	600	20	600	20	600	20	600
Delay A => PAD	16.80	60.68	17.08	60.96	18.81	67.97	19.11	68.06
Slew A => PAD	22.47	60.02	22.19	60.03	23.44	72.83	22.89	72.78

Case C: St0 = 0 / St1 = 1

	Rise				Fall			
Slope [ns]	0.1		2		0.1		2	
Load [pF]	20	600	20	600	20	600	20	600
Delay A => PAD	20.01	76.95	20.29	77.22	22.34	85.24	22.70	85.33
Slew A => PAD	30.11	63.34	29.91	63.43	31.64	78.05	31.22	77.99

Case D: St0 = 1 / St1 = 1

	Rise				Fall			
Slope [ns]	0.1		2		0.1		2	
Load [pF]	20	600	20	600	20	600	20	600
Delay A => PAD	23.11	91.65	23.39	91.93	23.51	100.36	24.04	100.44
Slew A => PAD	35.34	69.70	35.14	69.98	37.95	85.73	37.52	85.63

Operating Modes

Variation of the Slew-Rate

With the two Slew-Rate Control Input signals St0 and St1 four different slew-rates can be selected A, B, C, and D. Figure 1 shows an example of the four different output signals for the settings of the Slew-Rate Control Input signals. For the simulation an external capacitance of 100pF was used.

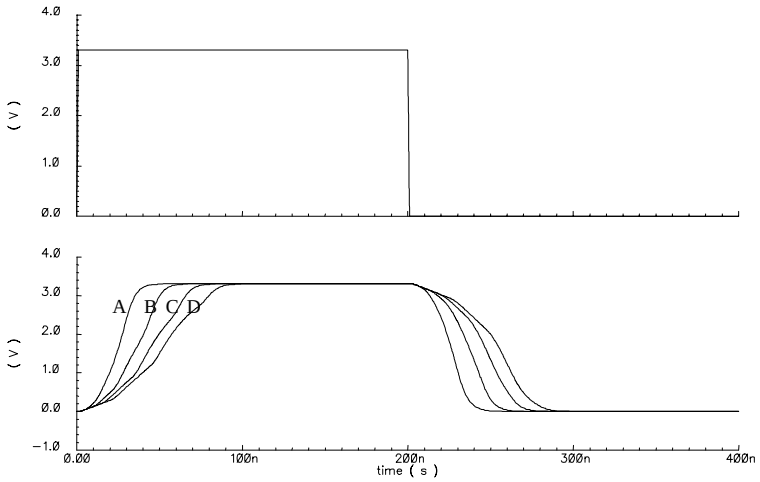

Figure. 1: Variation of the slew-rate of the output signal (St0, St1 settings)
(**above**: input signal, **below:** output signals)
Case A: St0 = St1 = 0 (slew-rate 1 / highest)
Case B: St0 = 1 / St1 = 0 (slew-rate 2)
Case C: St0 = 0 / St1 = 1 (slew-rate 3)
Case D: St0 = St1 = 1 (slew-rate 4 / lowest)

Independence of the Output Signal from Rise and Fall Time Variations of the Input Signal

Figure 2 shows that the waveform of the output signal is independent of variations of the rise and fall time of the input signal. As the input signals often have different rise and fall times, depending on the design of the core logic, the independence of the output signal is another advantage of the BU8SRC Slew-Rate Controlled Output Buffer. The upper waveforms show the rise and fall times of the input signal varied in the range from 1ns to 100ns. The waveforms below show that the slew-rate of the output signals remains nearly the same.

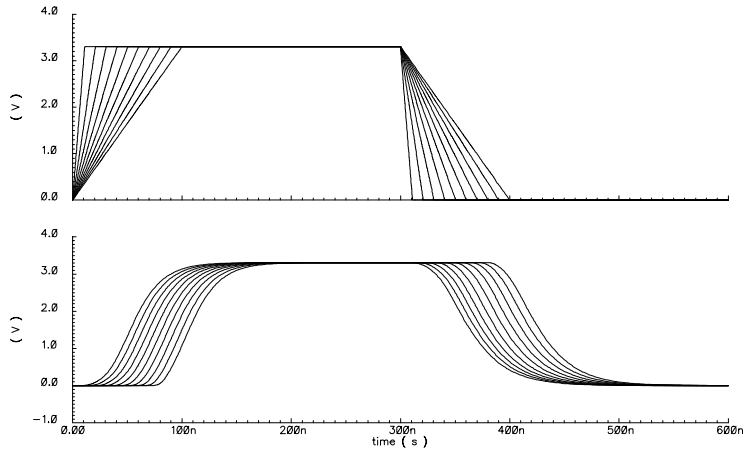

Figure 2: Input rise and fall time variation compared to the slew-rate of the output signals (input signal: tr = tf = 1ns…100ns)

Rise and Fall Time versus External Capacitance

Different external load capacitances cause different rise and fall times of the output signal. The rise and fall times of the output signal for the four possible Slew-Rate Control Input signals settings versus the output capacitance are shown in figures 3-6.
In this case the output capacitance was varied from 1pF to 500pF.

Case A: St0 = 0 / St1 = 0

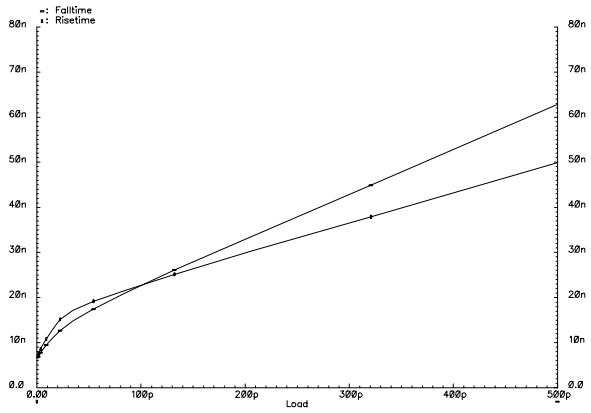

Figure 3: Rise and fall time vs. output cap. (St0 0 / St1 = 0)

Case B: St0 = 1 / St1 = 0

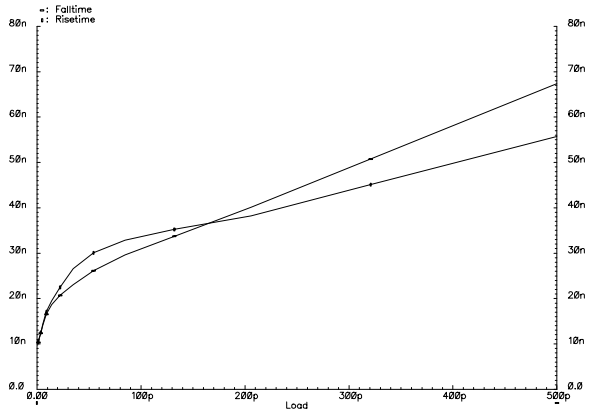

Figure 4: Rise and fall time vs. output cap. (St0 = 1 / St1 = 0)

Case C: St0 = 0 / St1 = 1

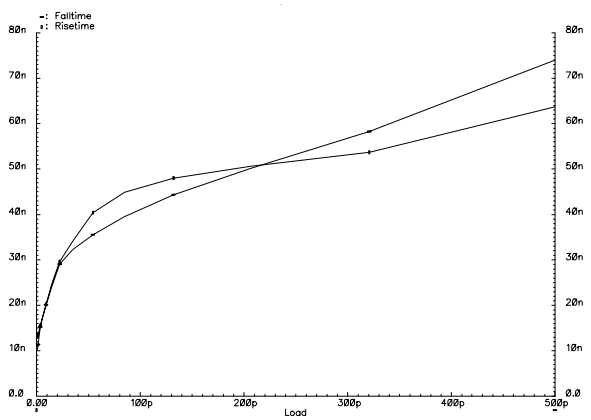

Figure 5: Rise and fall time vs. output cap. (St0 = 0 / St1 = 1)

Case D: St0 = 1 / St1 = 1

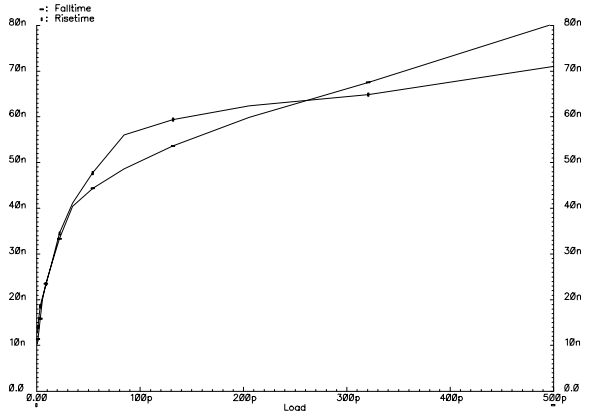

Figure 6: Rise and fall time vs. output cap. (St0 = 1 / St1 = 1)

Typical Application

The BU8SRC Slew-Rate Controlled Output Buffer is targeted at IC designs where the reduction of the conducted and radiated electromagnetic emissions of integrated circuits is of crucial importance.

Contact

austriamicrosystems AG
A 8141 Schloss Premstätten, Austria
T. +43 (0) 3136 500 5971
F. +43 (0) 3136 500 5755
emc@austriamicrosystems.com

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